

# Achieving ZVS in a Two Quadrant Converter Using a Simplified Auxiliary Circuit with Novel Control

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**Abstract-** This paper proposes a new soft-switching scheme as well as a novel control approach for a two quadrant converter. The auxiliary engine utilizes a simple architecture consisting of pair of switches, an inductor and several diodes to provide the necessary characteristic. We propose a simple two-quadrant current feedback scheme that adjusts the auxiliary switch on-times appropriately to minimize conduction losses, thus achieving ZVS in both quadrants from maximum negative to maximum positive load. Dead-time is fixed but conduction time of the auxiliary switches occurring within the dead-time is variable with load. A brief survey of various conventional techniques is also presented. PSIM simulations for the proposed model as well as a unique MathCAD analysis of the various states along with empirical data are provided.

## I. INTRODUCTION

Generally, for applications involving a 2-quadrant drive, zero voltage switching (ZVS) is achieved by the use of an Active Resonant Commutated Pole Converter [1] or any of its variants [2-7]. The basic concept of this converter is shown in Figs 1 and 2. Essentially, auxiliary switches SX1 and SX2 provide a resonant charge and discharge of the two main switches through Lx in order to achieve the desired ZVS characteristic. This is necessary in order to overcome any freewheeling current that is normally directed to the anti-parallel body diodes associated with the main switch MOSFETs.

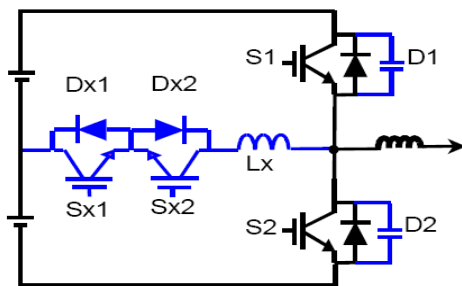


Figure 1. Active Resonant Commutated Pole Converter (ARCP)

Such a circuit is not only advantageous from an efficiency standpoint, but is also excellent from a noise perspective. This is due to the fact that this resonant circuit practically eliminates the reverse recovery issue that is associated with the main switch body diodes. In order to explore how this issue arises in a hard switched converter, let's take the case when the load current is positive, or in the direction shown in the arrow in Fig. 1, starting with the high side switch in the on-state. Once this high switch turns off, assuming the current is high enough, the MOSFET output capacitances discharge to zero and the low side switch's anti-parallel body diode resumes full load conduction during the subsequent dead-time. Interestingly depending on the load, the lower MOSFET may turn on under a ZVS condition. After the

dead-time ends, the lower MOSFET turns on and shunts the load current flowing through its body diode. Eventually the lower MOSFET turns off and the load current resumes back into its body diode once again. So far there is no issue of course until this particular dead-time interval ends and the upper MOSFET turns on. Here the upper MOSFET turns on hard and forces the body diode of the lower MOSFET to turn off sharply. Depending on the size of the load, and the type of MOSFET used, there may be a significant body diode recovery loss. Also, if the MOSFETs are large, the output capacitances will be significant and there will be high peak charging currents as well. Apart from risk of damage of the lower MOSFET's body diode, the resulting current spike and extra heat dissipation could prove fatal in a low noise, high efficiency requirement. To sum up, if the inductor current is positive (buck or "motoring phase"), the bottom MOSFET body diode freewheels during the dead-time and exhibits recovery loss once the top MOSFET turns on. Conversely if the current is away from the load, or negative (boost or "regenerative phase"), the top MOSFET body diode freewheels with recovery loss upon turn on of the bottom MOSFET. The purpose of the auxiliary circuit is to softly redirect this freewheeling or load current away from the body diodes and towards the auxiliary switches during the dead-times to such an extent that the voltage seen across these main switches is zero right before turn on. Here we relieve the current flowing through either MOSFET body diode as well as to sufficiently charge or discharge the respective MOSFET output capacitances prior to turn on. A split voltage in the conventional ARCP is necessary to sufficiently reset the snubber inductor during the main switch conduction interval. It is important to ensure reset of this snubber inductor to minimize the losses incurred in the auxiliary FETS which is a requirement for these devices to achieve ZCS (zero current switching). Ideally, snubber losses are mainly incurred during the commutation interval. This technique, as evident in Fig. 1, consists of two series capacitors, a resonant inductor as well as a 4-quadrant switch. Here, complexity is an issue when taking into account the required control and drive circuitry as well.

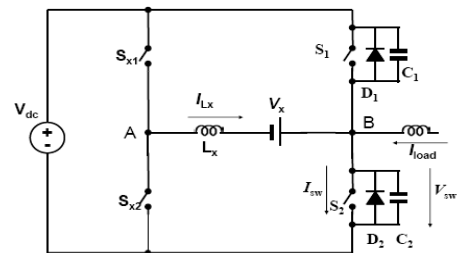


Figure 2. Equivalent ARCP Circuit

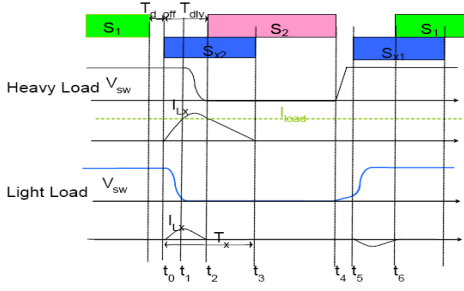


Figure 3. ARCP Timing Waveform

## II. COUPLED INDUCTOR

A popular variation of the ARCP, called the “coupled inductor approach” is shown in Fig. 4 [8]. Though the snubber choke is more complicated, overall complexity is somewhat reduced relative to the conventional ARCP scheme. This approach uses a simpler and more conventional auxiliary FET drive scheme. The four-quadrant switch and split capacitors are replaced with a two-quadrant switch, a slightly more complicated choke and a pair of diodes. Thus the drive complexity for this topology is significantly reduced. Resonant inductor reset is provided with the help of the coupled winding through diodes DX1 and DX2. The drawback here is that for a turns ratio of 1:1, the effective source voltage for the resonant circuit is  $\frac{1}{2}$  of  $V_{dc}$ . Thus it is required here to boost the resonant choke current to a level equal to the load current prior to turn off of the main switch. It also generally requires variable timing control in order to minimize the losses at light load. To remedy this, there is a technique that uses fixed timing control however with a non-unity turns ratio [9]. Here,  $S_{x1}$  and  $S_{x2}$  are respectively commutated during alternate dead times. When  $S_{x1}$  is activated in the motoring or buck phase, the snubber choke current,  $I_{(snub)}$ , is charged to the extent that the  $D_2$  current, or load current is supplied through the  $S_{x1}$ - $L_s$ - $T_1$ - $D_2$  path. This eventually turns  $D_2$  off and subsequently charges  $C_1$  and  $C_2$  resonantly to the point where  $D_1$  conducts.

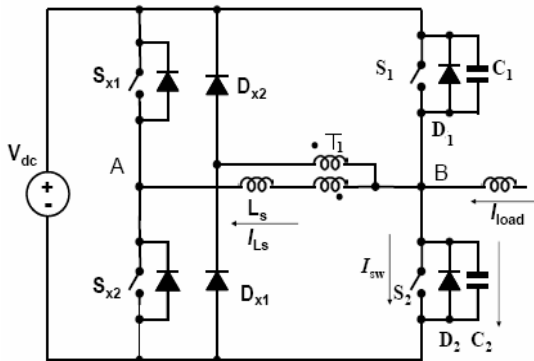


Figure 4. Coupled Inductor Approach

Main switch  $S_1$  is then commanded to turn on under a zero voltage condition. A short period of time later,  $S_{x1}$  turns off and the coupled inductor,  $L_s$ , freewheels through  $D_{x1}$  against a reset voltage provided by the coupled winding.

Assuming we’re still in the buck phase, during the next dead-time interval,  $S_{x2}$  turns on and  $L_s$  resonantly discharges  $C_1$  and  $C_2$  to the extent that node “B” in Fig. 4 clamps to zero via  $D_2$  before main switch  $S_2$  is commanded on. It is important to note here that the load current has the tendency to freewheel into the bottom MOSFET body diode and thus helps in discharging node “B” as well. This is one reason for the asymmetry associated with the resonant inductor current waveform. In essence,  $S_{x2}$  provides help to the load in order to achieve ZVS of the bottom switch in “buck” mode. Thus, the auxiliary switch  $S_{x2}$  does more work at no load rather than full load. It is important to note that the discharge path here is  $C_1/C_2$ - $T_1$ - $L_s$ - $S_{x2}$ .

The “regenerative” mode is an entirely different case. Here the load current is negative and flows into the switches as shown by the arrow in Fig. 4. The supply in this mode behaves as a boost converter where the  $S_2$  acts as a switch and  $S_1$  a boost diode. In a programmable supply, the load current may be negative during quick output voltage down-programming due to the discharge of the output capacitance. In fact, this is typical for a medical ultrasound product. Here, this output capacitance can be on the order of 65 $\mu$ F with a required output slew of 200V to within 1mS. However this is considered a transient condition and ZVS may not be necessary in this mode. This would preclude the use of auxiliary switch,  $S_{x2}$  altogether. However, in DC motor applications that require regenerative braking, the motor behaves as an electric generator. In this case kinetic energy is converted into electrical energy and transferred back into the supply bus. Thus the current through the output inductor is clearly negative or towards the main switches in the steady-state. It is interesting to note that in this case the load current isn’t helping the auxiliary switch  $S_{x2}$  to achieve ZVS of the bottom switch as was true in the former case. Auxiliary switch  $S_{x2}$  must do significantly more work in this mode. Therefore the timing control logic for regenerative mode must take this into account.

## III. SINGLE INDUCTOR APPROACH

An even simpler approach shown in Fig. 5 which has been proposed in motor drive applications [10] utilizes a single inductor and two auxiliary switches. This approach overcomes the complex choke used in the previous approach. The auxiliary switches work in the same fashion as before however reset of the resonant inductor,  $L_{sn}$ , is achieved through the body diodes of the auxiliary MOSFETS. The only disadvantage for this approach is the detrimental effect associated with the auxiliary MOSFET output capacitances. Here, simulations show that this capacitance can cause significant residual current in the auxiliary MOSFET body diodes due to insufficient reset of the resonant choke. The PSIM

simulation shown below illustrates this effect with a auxiliary MOSFET capacitance of only 400pF each. Depending on the application, this may not be an issue however the ZCS nature of the auxiliary circuit is lost resulting in higher noise and loss. For motor drive applications this is likely not an issue however.

Fig. 6 shows a PSIM simulation of Fig. 5. The top plot in Fig. 6 shows the snubber choke current. Here we see a residual current of roughly 5 Amps into each auxiliary switch due to insufficient reset. Here this current can flow throughout the entire conduction time of the main switches since there is no longer a voltage drop across the snubber choke to allow any additional reset. The middle plot shows the source voltage of the main switch S1 (with ZVS) and the bottom plot shows the control signals for all four MOSFETS. Vhigh and Vlow are the main switch logic signals and Vsnhigh and Vsnlow are the auxiliary switch control signals.

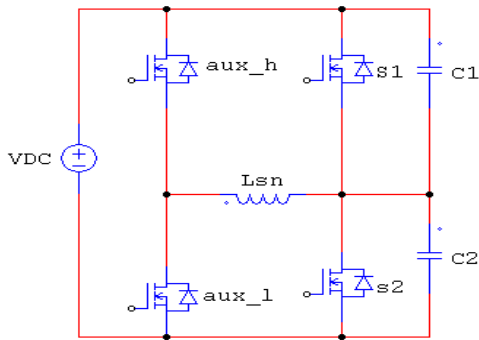


Figure 5. Single Inductor Approach

#### IV. PROPOSED APPROACH

A simple technique, and the one proposed in this paper, overcomes the ill effects of the single inductor approach discussed previously. This circuit shown in Fig. 7 appears

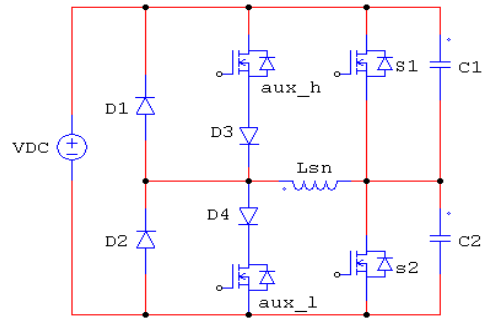


Figure 7. Proposed Approach

For the example cited in this paper, this converter's input is fixed at 340V with an output voltage programmable voltage range of 30V to 210V. Not shown in the above figure is the converter's output filter.

to be a good compromise between the coupled inductor approach and single inductor approach. Here we still use the single inductor, as in the former case, but also use diodes D1- D4 as well. The advantage is near perfect reset of the resonant inductor while maintaining simplicity of design. The circuit behaves similarly to the previous approach however the reset mechanism for Ls is directly through D1 and D2. Here we do not have the benefit of a reset voltage as before with T1 in the coupled inductor approach during the main switch on times.

It is interesting to note that right after turn off of either of the auxiliary switches, the resonant choke current, ILsn, rapidly ramps down towards zero through natural inductive kickback. Here, the full rail voltage, Vdc, is impressed across the resonant choke during this interval.

To get an idea of the benefit of this circuit, we will explore the operation during resonant charge of the main switches as well as resonant discharge as shown in Fig. 8. The top trace in the figure is the source voltage of the top main switch, S1 (with perfect ZVS). The second trace represents main and auxiliary switch timing signals with

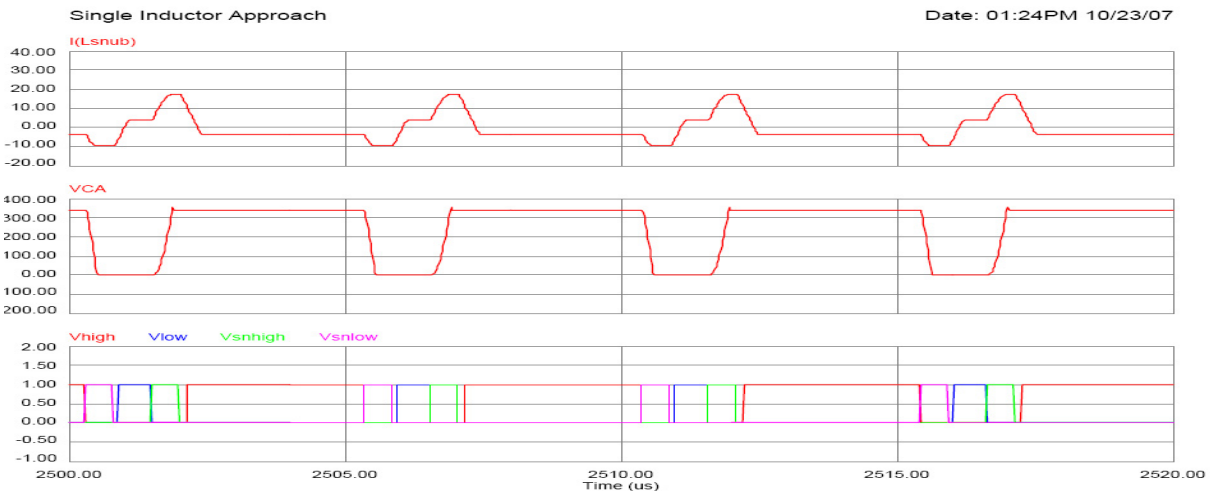


Figure 6. PSIM of Single Inductor Approach

Note: The waveforms in the figure show perfect ZVS (Vca). However it also shows the ill effect of insufficient reset in the auxiliary choke IL(snub). This current flows through the auxiliary FET body diodes and in this particular case is as high as 5A. The conditions of this simulation are as follows: Vout=250V; Iload=5A, Vdc=340V, C1 and C2=400pF; Ls=6uH, d=74%.

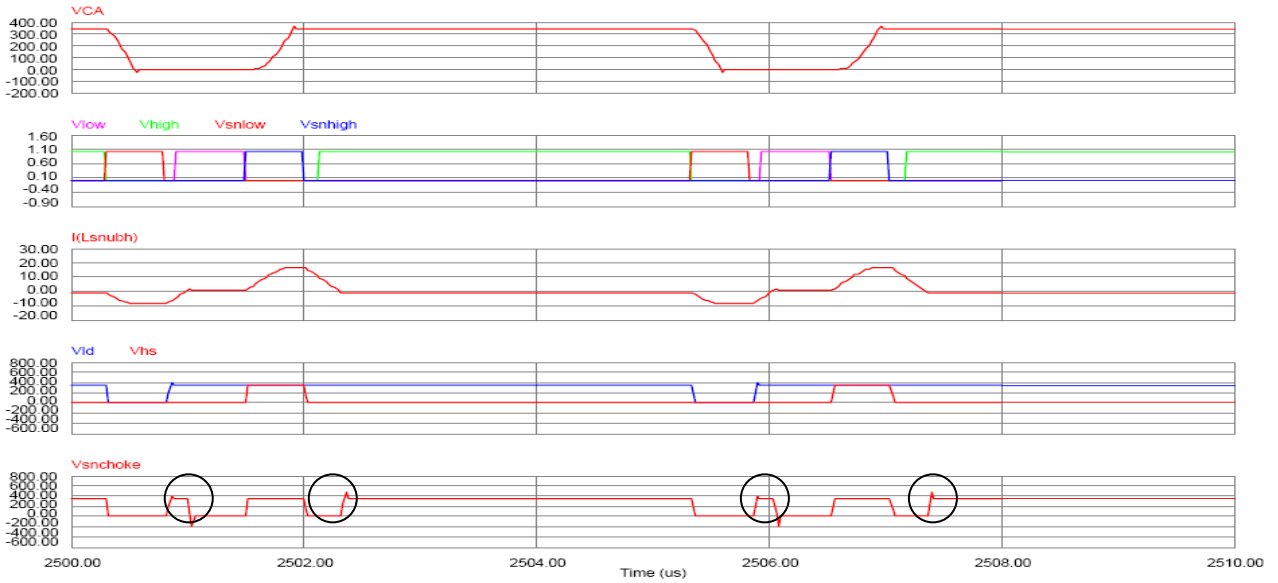


Figure 8. PSIM of Proposed Design

Note: The circled regions show the rise or fall of the of the snubber choke voltage right after the snubber current crosses Zero. A capacitance present at Vschoke will slow this rise and fall to the extent that a non-zero current exists in the choke throughout the entire aux switch conduction interval.

Vhigh and Vlow representing the main switches and Vsnhigh and Vsnlow the auxiliary switches as before. The third trace represents the snubber choke current  $I(L_{snubh})$  and the fourth trace shows the source voltage of the top aux FET and the drain voltage of the bottom aux FET. Finally, the last trace shows the snubber choke drive point or the cathode of D3.

We start with the bottom switch, S2, in the on state in “buck” mode. Once S2 turns off, its body diode takes over and conducts the full load current. The top aux FET then turns on and takes over by supplying the full load current through Lsn. Body diode of S2 now turns off allowing the main switches to resonantly charge towards the input rail. Eventually the body diode of S1 conducts with the main switch S1 turning on shortly thereafter with ZVS. The top aux FET now turns off and resets. Its output capacitance is discharged through D3 during reset and is clamped by D2. The resonant choke current thus resets rapidly towards ground. Once the current goes to zero there is no energy left in the choke so it naturally wants to rise towards Vdc instantly (note the circled regions in Fig. 8 correlated with the aux FET voltages in the preceding trace). This is not exactly possible due to the parasitic capacitances of D1, D2, D3 and D4. The capacitances are relatively small and it is interesting to note that the large top and bottom aux FET output capacitances have now been successfully decoupled from the circuit. The effect is near perfect reset of the resonant choke.

On the other hand, a large capacitance present across D1 and D2 would result in a significant residual current in the aux FETS. This of course would be equivalent to the circuit in Fig. 5, and would result in unnecessary

conduction loss. This is why it’s necessary to isolate the auxiliary MOSFET output capacitances. Here the MOSFET output capacitors are effectively blocked by D3 and D4 during the points of interest. Nonetheless, it should be noted that even with very low effective capacitance of D1 and D2, we still do not have perfect reset due to the parasitic capacitance of the diodes. Our simulation model assumes that this capacitance is 100pF per diode.

Conditions for the simulation are as follows:

Vout=250V; Iload=5A, Vdc=340V, C1 and C2=4000pF (Cres=8Kpf); Ls=6uH, d=74%. Junction capacitance of D1 and D2=100pF. Aux1 and Aux 2 MOSFET output capacitance=4000pF. Note the command logic for the following switches: Vlow=S2; Vhigh=S1; Vsnhigh=Aux\_h; Vsnlow=Aux\_low.

## V. RELEVANT EQUATIONS

In order to determine the various expressions that govern the proposed circuit, we must understand the various states of operation.

Here we assume “buck” mode and determine that there are a total of six states. Before we proceed with analyzing these states, the following equations (1-3) apply.  $L_{snubber} = L_{sn}$ .

$$I_n = V_{dc} / Z_o \quad Z_o := \sqrt{\frac{L_{snubber}}{C_{res}}} \quad (1) \quad (2)$$

$$wr := \frac{1}{\sqrt{L_{snubber} \cdot C_{res}}} \quad (3)$$

For the first interval, we start out with high side switch, S1, turning off and with body diode D2 subsequently conducting full load current at the commencement of the dead-time interval. Low side switch, S2, then turns on. After the S2 conduction time expires, the body diode of S2 again conducts the load. At this moment auxiliary switch, aux\_h, turns on. This interval ends when the D2 current goes to zero thereby allowing the drive to charge. The duration of this time is shown in (4). Here we assume that the recovery current is negligible.

$$0 < t < t_{01} \quad t_{01} := \frac{I_{load} \cdot L_{snubber}}{V_{dc}} \quad (4)$$

The next interval begins at time  $t_{01}$ . This is where the capacitors, C1 and C2 resonantly charge towards the input rail,  $V_{dc}$ . At the end of this interval, the body diode of the top MOSFET should clamp with a peak current of  $I_{pk}$  into  $V_{dc}$  as given in (1). The time duration of this interval is given in (5) with (6) representing the voltage on the main switches and (7) representing the current through the resonant choke.

$$t_{01} < t < t_{01} + t_{12} \quad t_{12} := \frac{1}{\omega r} \cdot \arcsin \left( \frac{V_{dc}}{I_n} \cdot \sqrt{\frac{C_{res}}{L_{snubber}}} \right) \quad (5)$$

$$V_{dc} - I_n \cdot \sqrt{\frac{L_{sn}}{C_{res}}} \cdot \cos[\omega r \cdot (t - t_{01})] \quad (6)$$

$$I_n \cdot \sin[\omega r \cdot (t - t_{01})] + I_{load} \quad (7)$$

The next interval begins at  $t_{01} + t_{12}$ . This is the ideal moment to turn on high-side main switch in order to obtain ZVS. This is also good time to turn off the high-side auxiliary switch in order to allow for the reset of the resonant choke. It should be noted that the value of  $t_{01} + t_{12}$  is dependant on several parameters such as load current, resonant capacitance, input voltage and resonant inductance. However, the load current is the only parameter that is expected to vary. All other parameters can be treated as constants in determining the precise moment of when to turn on the top main switch. The main switch voltage at  $t_{01} + t_{12}$  is  $V_{dc}$  all the way up to  $d \cdot T_{sw}$  (full high-side conduction interval).  $V_c(t)$  is defined as the main switch drive point, “d” as the duty cycle and  $T_{sw}$  the switching period. Additionally, the resonant choke current is expressed in (8) below. As can be observed in (8), the resonant choke must supply the

$$t_{01} + t_{12} < t < dT_{sw}$$

$$I_n \cdot \sin[\omega r \cdot (t_{12})] + I_{load} - \frac{V_{dc}}{L_{sn}} \cdot (t - t_{01} - t_{12}) \quad (8)$$

full load current in addition to the resonant current needed to charge the main switches. This current decreases linearly with time until it reaches zero.

The next interval begins at the end of the top main switch conduction cycle, or at  $d \cdot T_{sw}$ . At this moment we resonantly discharge the main switch output capacitances through the bottom auxiliary switch. Expression (9) quantifies the minimum on-time necessary for the bottom auxiliary switch to achieve perfect ZVS. The expression within the parenthesis in (9) is the main switch voltage,  $V_c(t)$ . As expected, this on-time is inversely related to load current. The more load we have the lower the on-time requirement for this switch. Also note that (9) uses a MathCAD “root” function (with an initial guess value of 0.1 uS we let MathCAD solve). The resonant choke current in this interval goes negative and is expressed in (10). Note that it does not contain load current as it had in (7) which explains the asymmetry. Note that (9) is a simplification (see end of section VII).

$$dT_{sw} < t < dT_{sw} + t_{23}$$

$$t_{23} := \text{root} \left( V_{dc} \cdot \cos(\omega r \cdot t_d) - \frac{I_{load}}{C_{res}} \cdot t_d, t_d \right) \quad (9)$$

$$-I_n \cdot \sin[\omega r \cdot (t - dT_{sw})] \quad (10)$$

The final interval begins when the bottom main switch turns on. The optimal time for this to happen is  $d \cdot T_{sw} + t_{23}$  and should last until  $T_{sw}$ . Here  $V_c(t) = 0$  and the resonant choke current,  $I_L(t)$  ramps down to zero via the input rail,  $V_{dc}$ .

## VI. MATHCAD SIMULATION

A convenient way of capturing all of the equations is to construct a MathCAD “conditional if array” for both the main switch drive point (11) and the resonant choke current (12). From these expressions, single cycle plots can easily be obtained ( $I_{ld} = I_{load}$ ,  $C_r = C_{res}$ ). The plots are shown in Figs 9 and 10 with  $V_{dc} = 340V$ ,  $L_s = 6\mu H$ ,  $C_r = 8000pF$ ,  $V_o = 250V$  ( $d = 74\%$ ),  $I_{load} = 5A$  (same conditions used in PSIM simulation in Fig. 8). Note that (11) and (12) contain MathCAD statements that account for the diode clamping effect of the resonant choke current as well as the resonant voltage clamping above  $V_{dc}$  and below ground. Note the very good correlation between the MathCAD plots and the PSIM simulation. This method proves to be an extremely fast and interactive way of seeing how load current, or any other relevant parameter, can affect the result. Note the excellent correlation of Figs 9 and 10 with the PSIM result shown in Fig. 8.

$$V_c(t) := \begin{cases} 0 & \text{if } 0 < t < t_{01} \\ V_{dc} - \text{In} \cdot \sqrt{\frac{L_s}{C_r}} \cdot \cos[\omega r(t - t_{01})] & \text{if } t_{01} < t < t_{01} + t_{12} \\ V_{dc} & \text{if } \text{In} \cdot \sqrt{\frac{L_s}{C_r}} \cdot \sin[\omega r(t - t_{01})] > V_{dc} \\ 0 & \text{if } \text{In} \cdot \sqrt{\frac{L_s}{C_r}} \cdot \sin[\omega r(t - t_{01})] < 0 \\ V_{dc} & \text{if } (t_{01} + t_{12}) < t < dT \\ V_{dc} \cos[\omega r(t - dT)] - \frac{I_{Ld}}{C_r} (t - dT) & \text{if } dT < t < dT + t_{23} \\ 0 & \text{if } t > dT + t_{23} \end{cases} \quad (11)$$

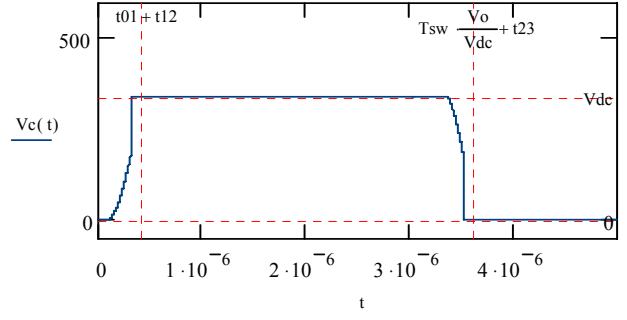


Figure 11. Non perfect case: This signal represents (11) with  $T_{a\_H}$  (250ns)  $< t_{01}+t_{12}$  and  $T_{a\_L}$  (150ns)  $< t_{23}$ . Thus the main switches turn on prematurely.

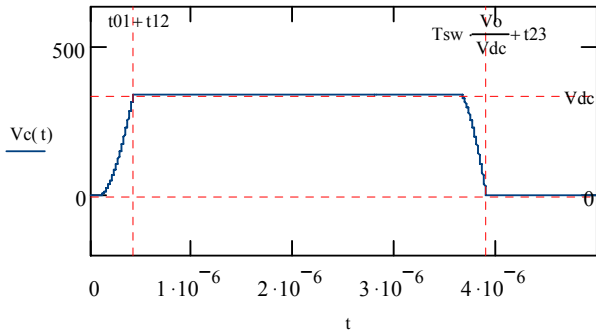


Figure 9. MathCad of Main Switch Voltage

Note the resonant charge of the main switch voltage. The discharge is aided by the load current when in “buck mode”. We have perfect ZVS.

$$I_L(t) := \begin{cases} \frac{V_{dc}}{L_s} \cdot t & \text{if } 0 < t < t_{01} \\ \text{In} \sin[\omega r(t - t_{01})] + I_{Ld} & \text{if } t_{01} < t < t_{01} + t_{12} \\ \text{In} \sin[\omega r(t_{12})] + I_{Ld} - \frac{V_{dc}}{L_s} (t - t_{01} - t_{12}) & \text{if } t_{01} + t_{12} < t < dT \\ 0 & \text{if } \frac{V_{dc}}{L_s} (t - t_{01} - t_{12}) > \text{In} \sin[\omega r(t_{12})] + I_{Ld} \\ -\text{In} \sin[\omega r(t - dT)] & \text{if } dT < t < dT + t_{23} \\ \frac{V_{dc}}{L_s} (t - dT - t_{23}) - \text{In} \sin[\omega r(t_{23})] & \text{if } dT + t_{23} < t < T \\ 0 & \text{if } \frac{V_{dc}}{L_s} (t - dT - t_{23}) > \text{In} \sin[\omega r(t_{23})] \end{cases} \quad (12)$$

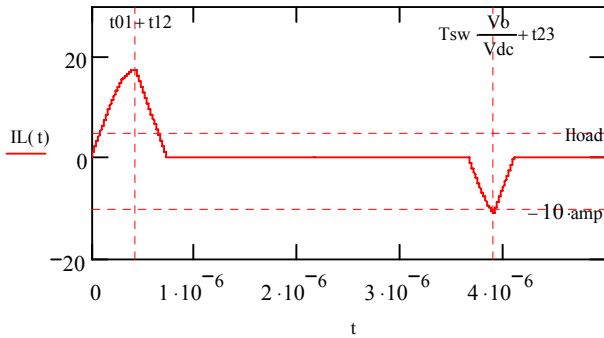


Figure 10. Resonant choke current-Ideal case (perfect ZVS).

## VII. PROPOSED CONTROL LOGIC

There has been a significant amount of research done on ZVS control. For example there is fixed dead-time control [11] and variable control [12] among others [13]. The method proposed here utilizes a fixed dead-time however with variable auxiliary switch on-time that is keyed to load current as shown in Fig. 12. The technique presented here works in both quadrants.

To start with our control logic, we write the expressions, (13) and (14), to determine the auxiliary switch on-times and plot those against load current for both negative and positive load as shown in Fig. 12. Once again we use conditional if statements to determine the aux on-times. Quadrant II on-times (negative load case) are simply mirror images of the quadrant I expressions (4), (5) and (9). These curves will be useful in determining the control logic timing for the auxiliary switches. Thus we will need circuitry that is keyed to the output load current via the relationship shown in the Fig. 12. We must ensure that the on-times of the respective auxiliary switches start at the same point at zero load and move in the direction shown in the figure. We also need to ensure that, at maximum load, there's enough ZVS pulse-width to accommodate the maximum aux switch on-time requirements shown in Fig. 12. A summary of the control logic diagram and waveforms are shown in Fig.'s 13 and 14.

$$T_{auxL}(I_{load}) := \begin{cases} t_{01}(-I_{load}) + t_{12} & \text{if } I_{load} < 0 \\ \text{root}\left(V_{dc} \cos(\omega r \cdot t_d) - \frac{I_{load}}{C_{res}} \cdot t_d, t_d\right) & \text{if } I_{load} \geq 0 \end{cases} \quad (13)$$

$$T_{auxH}(I_{load}) := \begin{cases} t_{01}(I_{load}) + t_{12} & \text{if } I_{load} \geq 0 \\ \text{root}\left(V_{dc} \cos(\omega r \cdot t_d) - \frac{-I_{load}}{C_{res}} \cdot t_d, t_d\right) & \text{if } I_{load} < 0 \end{cases} \quad (14)$$

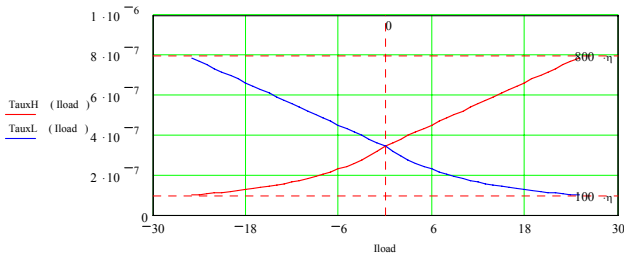


Figure 12. Optimum Auxiliary Switch On-times

In Fig. 12 we show the required on-times for each auxiliary switch for both positive and negative load currents in order to achieve ZVS. As expected, at zero load, both switches have the same on-time requirement. This is due to the fact that there is no load current to skew the symmetry. With negative load, the top main switch is clamped to the rail by the load current thus requiring more work for the bottom aux switch. At positive load, the bottom main switch is clamped to zero requiring the top aux switch to do more work.

A control block diagram is shown in Fig. 13. The current amplifier shown is intended to detect positive or negative load current. The output swing should be limited to +/-5V for full scale load variation. The purpose of the offset, whose level should equal to the maximum negative value of the current amplifier output, is to shift this signal appropriately such that the comparators always see positive voltage. Again, the circuit must ensure that the requisite ZVS pulse width is achieved at maximum load.

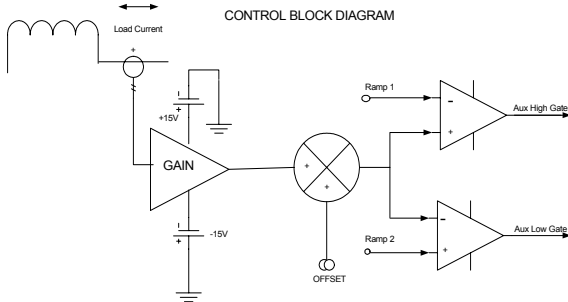


Figure 13. Proposed Control Block

The timing waveforms necessary for ZVS are shown in Fig. 14 below. The “load current” signal shown here incorporates the offset shown in Fig. 12. Thus at zero load this signal should be centered between ramps 1 and 2. The size of these ramps should depend on the results obtained in (13) and (14). Note that the auxiliary switches turn off right before either the top or bottom main switch activates to prevent the main switch drive point from resonantly riding away from the ZVS condition.

The proposed analog control logic represented in Figs 13 and 14 will reasonably approximate the curves generated

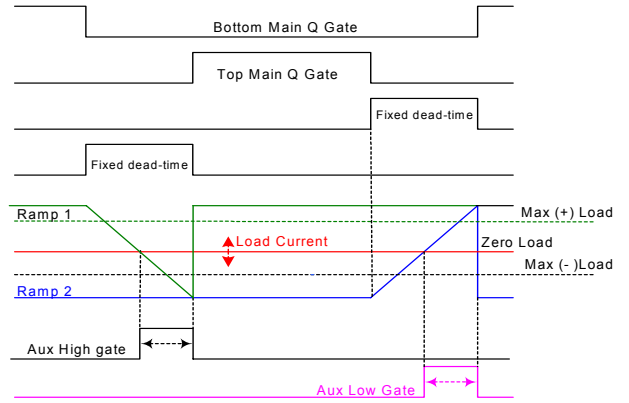


Figure 14. ZVS Timing Waveforms

in Fig. 12. The zero load on-times of the respective aux switches is  $= (T_{on\ Max-} - T_{on\ Min})/2$  or 450nS. This is slightly skewed from the ideal value of 380nS given in the figure.

It should be noted that the on time curves appear to asymptotically approach a finite value at the low end. This is because the “root” calculation in (9) assumes the load current and the aux switch discharges the main switches right at the start of the dead-time. Therefore this value represents how long it will take for the main switch voltage to reach zero with the load current and aux switch working simultaneously. This is somewhat different than what the actual case will be. Here, the load current discharges the main switches prior to activation of the aux switch (see timing in fig. 14). A small time later the aux switch will turn on and help to load in providing ZVS. Thus contrary to the curves shown in fig. 12, it’s conceivable that with high enough load current the either aux switch on time requirement reaches zero.

## VIII. EXPERIMENTAL RESULTS

We will compare a MathCad simulation run with an output setting of 30V with a 7A load against actual values. This is the low end of the operational range of our two quadrant converter (30V -210V/ 210W max). This set-point also illustrates the maximum benefit that is obtained with this ZVS concept since the respective MOSFET currents will be at their highest levels in this design. *Conditions for the MathCad simulation are as follows:*  $V_{out}=30V$ ;  $I_{load}=7A$ ,  $V_{dc}=300V$ ,  $C_{res}=1500pF$ ;  $L_s=6\mu H$ ,  $d=8.8\%$ .

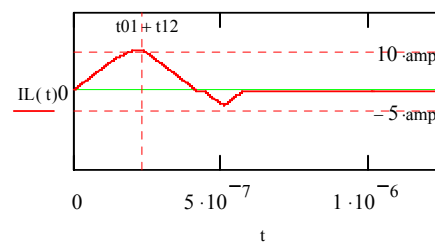


Figure 15. Resonant Inductor Current

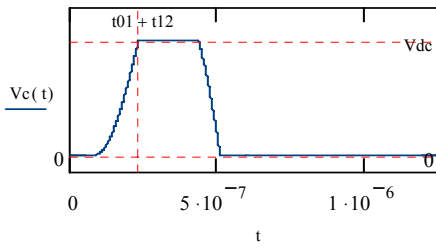


Figure 16. Main Switch Drive Point

Note: MathCad results:  $t_{01}+t_{12}=237\text{nS}$ ;  $t_{23}=73\text{nS}$ .

The following represents a scope waveform of both (11) and (12) under the same conditions as listed in the previous MathCad simulation. It should be noted that the MOSFETS used in all cases is the Fairchild FQA24N50F. Note the excellent correlation between calculated and empirical data.

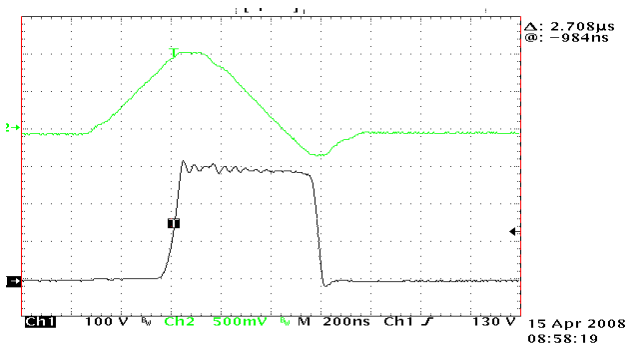


Figure 17-Actual Result

Top trace = Resonant Inductor Current 10A/Volt; Bottom trace = Main Switch Drive Point. Note also that  $t_{01}+t_{02}$  in the above photo appears to be roughly 250nS which is within 6% of the calculation of 237nS. The top trace current appears to peak out at 10A in the positive direction and 3A in the negative direction. This converges extremely well to the simulations of figs 15 and 16.

In addition, the next two photos shown in Figs 19 and 20 illustrate the operation of the circuit with variation in load.

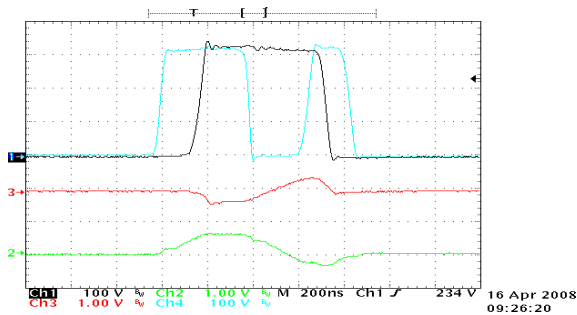


Figure 18-Relevant ZVS Waveforms

$V_{out}=30\text{V}$ ;  $I_{load}=3\text{A}$ ,  $V_{dc}=300\text{V}$ ,  $C_{res}=1500\text{pF}$ ;  $L_s=6\mu\text{H}$ ,  $d=8.8\%$ . Channel 1 (white trace) represents the main switch drive point. Channel 4 (blue trace) is the resonant drive point. Channel 3 (red trace) is the top main switch current at 10A/Volt and Channel 2 (green trace) represents the ZVS choke current at 10A/Volt.

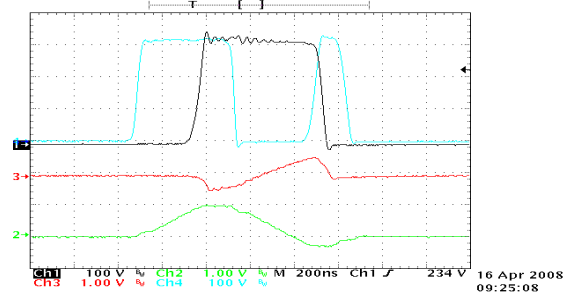


Figure 19-Relevant ZVS Waveforms

$V_{out}=30\text{V}$ ;  $I_{load}=6\text{A}$ ,  $V_{dc}=300\text{V}$ ,  $C_{res}=1500\text{pF}$ ;  $L_s=6\mu\text{H}$ ,  $d=8.8\%$ . Channel 1 (white trace) represents the main switch drive point. Channel 4 (blue trace) is the resonant drive point. Channel 3 (red trace) is the top main switch current at 10A/Volt and Channel 2 (green trace) represents the ZVS choke current at 10A/Volt. Note the wider gap between the ZVS and main switch drive points due to the higher load.

The next plot is an efficiency curve which compares ZVS against non-ZVS operation. At the higher current the efficiency difference becomes very significant. The total difference at maximum load approaches 14% which in this design would represent a difference of 75 Watts. Here our input is again 340V;  $C_{res}=1500\text{pF}$  and  $L_s=6\mu\text{H}$ . It should be noted that the efficiency is generally low since we are operating at 30V with 340V supply.

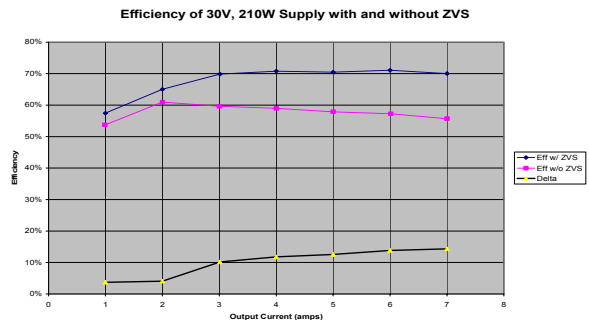


Figure 20-Efficiency vs. Load

## IX. CONCLUSION

A simple architecture which provides ZVS in a 2-quadrant drive was proposed. The new scheme provides simplicity of design over the more conventional approach in order to achieve ZVS. Near perfect reset of the resonant choke is also accomplished with the simple addition of several diodes. Simulations were done using PSIM and MathCad software which generated very similar results. Empirical data was also obtained which confirmed with very good accuracy a previous MathCad simulation. Additional photographs were included to illustrate the ZVS mechanism along with relevant currents at different load levels. Finally, efficiency was benchmarked against a non ZVS supply and the results appear very promising.

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